FROM PSEUDO-MOS TRANSISTOR TO A SOI-MOSFET WITH A NANO-CAVITY

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Abstract

The devices miniaturization pushes the SOI (Silicon On Insulator) technologies to some ultimate manufacturing techniques: buried oxides with a thickness spectrum from 400nm in the standard HTA SIMOX, down to tens of nm in Unibond technique. The paper comparatively presents the simulations of the electrical characteristics for a pseudo-MOS transistor and finally for an ultra-thin SOI transistor with a cavity. The influence of interface charges is accounted. If this charge is more important at upper interface in classical transistor with 200nm Si-film in insulator, the simulations reveal a higher contribution of the bottom interface charge in the nanotransistor case. The I_D-V_{DS} characteristics with minimum, provided by specialty software, describe a transition way from SOI devices toward Semiconductor On Insulator nanotransistors. A SOI nanotransistor with a cavity was proposed. The global current is a superposition of a tunnel current through the cavity and an inversion current at the film bottom. The tunnel source-drain current prevails in sub 1-nm film thickness and provides the I_D-V_{DS} characteristics with a minimum. For film thickness comprised between 200-10nm, the I_D-V_{GS} curves preserve similar shapes with a classical MOS/SOI's transfer characteristics.

Keywords: Transistors simulations, tunnel modeling, SOI, electrical characteristics

Presenting Author's biography

Cristian Ravariu. A short professional biography. Mr. Cristian Ravariu was born in Bucharest, Romania, in 1968. He studied in Bucharest, where he obtained the engineer degree in 1993, at Politehnica University of Bucharest, Faculty of Electronics and Telecommunications, Microelectronics Department.

He worked from 1993 to 1998 as Researcher at Institute of Microtechnology, Bucharest and from 1999 to this moment as Lecturer at Politehnica University of Bucharest.

In the last two years, due to the increasing interest in the nanotechnologies and stable and unstable quantum matter fields and due to his links with semiconductor physics, microtechnologies he researched these domains. A special passion for devices with biomedical applications, possible modeling in the living cells, he focused the efforts toward nanodevices and biodevices.

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1 General

The Single Electron Devices (SEDs) tend to become the main rivals for the sub-50nm classical CMOS devices. These ultimate CMOS dimensions, expected to be reached in 2014, are described as "high risk domain", due to the quantum effects, to be taken into account in the carriers transport.

In this paper the starting point is a standard SOI pseudo-MOSFET, with 200nm Si-film on 400nm Oxide. The $I_D(V_{DS}, V_{GS})$ curves were studied for thinner films:7nm, 2nm, 1nm, 0.3nm. Essentially, a new nano-structure, sub-3nm film thickness was proposed. The architecture was inspired from a real sub-10nm undulated polysilicon film, [1]. But the structure was modified to fulfil the Single Electron Transistor principle: one by one carrier transport from source to drain. We preserved just 2 "undulations" of Silicon onto an oxide support; thinning the Si-channel region, the carrier transport was confined at the limit, one by one. Essentially, the device could be regarded as a string of "Few Electron Transistors" that converges to the "Single Electron Transistor" (as an ideal limit). A specific nanodevice phenomenon, the tunnel current through a triangle potential barrier, was observed. Some electrons tunnel the Si - Vacuum barrier, producing the tunnel current, I_t [2].

2 The nano-device description

The device architecture, presented in fig.1, was inspired from a real sub-10nm undulated polysilicon film. We preserved just two high parallelepiped shape "undulations" of Silicon onto an oxide support. The source and drain regions are n^+-type silicon (N_D=10^{17}cm^{-3}) with z_{n+}=6nm, y_{n+}=7nm, x_{n+}=3nm, placed at x_c =3nm distance. A thinner p – type Si film (N_A=$5\cdot10^{15}$cm^{-3}) links the source and drain regions and represents the inversion channel location. All these parameters will be maintained constant during the simulations. Thinning the p-type film to y_{film}=1nm, than to 0,3nm, a cavity carried out between source and drain.

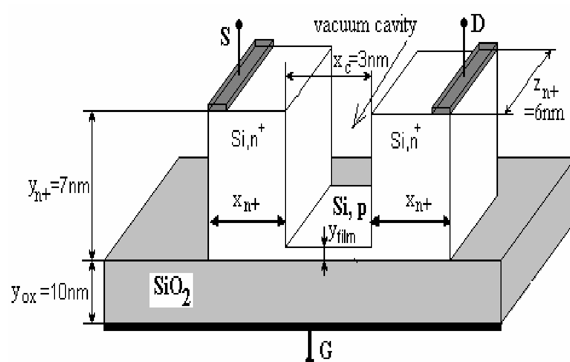


Fig. 1 The basic structure of the SOI nanotransistor.

The cavity could be optionally covered with an oxide layer (not presented in fig. 1, but presented in simulations). However the vacuum properties are fulfilled in nanocavity.

The device body is placed onto an oxide layer (y_{ox}=10nm). The substrate contact acts like a gate terminal. Because the vacuum distance is less than 4nm (x_c<4nm), then the probability of tunneling between n^+ - source to n^+ - drain meaningfully increases.

3 Analytical model

A specific nanodevice phenomenon, the tunnel effect through a triangle potential barrier, occurred. Some electrons tunnel the Si - Vacuum barrier, producing the tunnel current, I_t [2]:

$$I_t = \frac{A}{\sqrt{E_b}} \cdot \left(\frac{V_{DS}}{x_c}\right)^2 \cdot \exp\left(\frac{B \cdot E_b^{3/2} \cdot x_c}{V_{DS}}\right) \quad (1)$$

where $E_b = \chi_{semic} - \chi_{vacuum}$ is the height of the triangle barrier of the potential from semiconductor to vacuum and A, B are some material parameters depending on the effectiveness mass for electrons and holes, [2]. Zeroing the first order derivative of the model (1) results a minimum for the tunnel current versus V_{DS} voltage:

$$V_{DS}\big|_{I_t=\min} = \frac{B \cdot E_b^{3/2} \cdot x_c}{2} \quad (2)$$

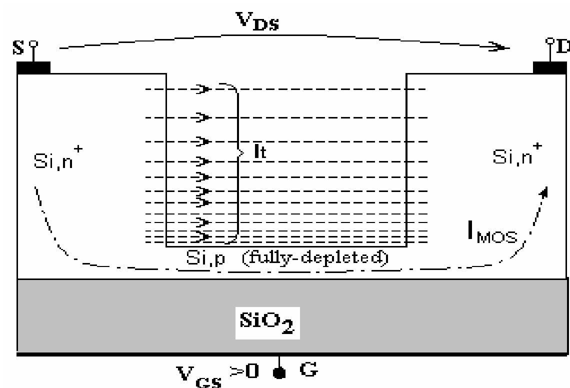


Fig. 2 The current flow in a cross-section.

The simulations proved that the total current presented this curvature with a minimum when the film thickness decreased under 1nm because the percentage of the tunnel current, I_t overcomes that from the inversion channel, I_{MOS}, fig.2. For thicker Si-p film (y_{film}>10nm), the tunnel current is negligible and the characteristics tend to those of the classical SOI-MOSFET. The cavity itself has a high vacuum. The number of air molecules N, in the cavity volume for y_{film}=1nm, is:

$$N = \frac{x_c \cdot (y_{n+} - y_{film}) \cdot z_{n+} \cdot N_A}{V_{m0}} \approx 2{,}8\text{molecules} \tag{3}$$

Consequently, the electrons weren't disturbed by the air from the cavity, in normal conditions (N_A=6,023×10^{23}molec/mol, V_{m0}=22,42dm^3/mol). So, the device doesn't require a special vacuum technology.

The Fowler-Nordheim tunneling probability of the electrons from semiconductor to vacuum is, [4]:

$$P_t \approx \exp\left[-\frac{4\sqrt{2m_n^*} \cdot \chi_S^{3/2} \cdot d}{3q\hbar V_{DS}}\right] \tag{4}$$

where m_n^* is the electron effective mass, χ_S is the semiconductor affinity for electrons in respect with the vacuum, ħ=h/2π (h is the Planck's constant), q is the elementary electric charge. In figure 5.a is presented the tunneling probability for two semiconductors: silicon and diamond, versus the drain-source voltage for the same vacuum distance, d=3nm. It is interesting that Diamond, that usually presents lower currents in respect with silicon because $E_{Gdiam}\approx 5\times E_{Gsi}$, here presents a higher tunneling probability because χ_{Si}=4,17eV and χ_{Diam}=7,2eV, [4]. Some simulations with Diamond film was presented, [5].

4 The simulation results

In the simulations with ATLAS, the constructive data were those described in paragraph 2. The "nano-effects" were simulated using ATLAS, taking into account the: Band to Band Tunnelling, Fowler-Nordheim tunnelling, Fermi distribution, including in the MODEL statement the following parameters: BBT, FNORD, FERMI. For comparisons, the voltages were the same: V_G= 0V…3V, V_D=0V…4V, V_S=0V, for all structures.

4.1 Pseudo-MOS transistor with 200nm film

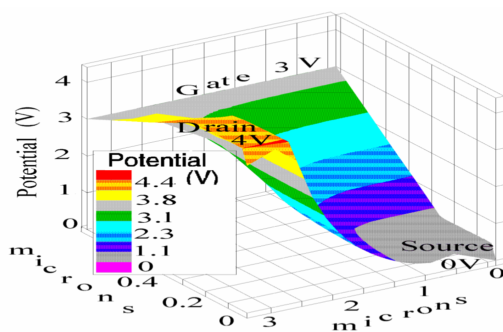


Fig. 3 The potential distribution in the 200nm structure.

The film thickness was varied. The simulations begin with a standard SOI 200nm Si / 400nm Oxide. Figure 3, 4 presents the potential distribution and the electron concentration in the structure with 200nm film thickness. A positive gate bias induces an electron inversion channel in p-type film (e.g. $n|_{y=0.2um} = 10^{16}\,cm^{-3} > 5\cdot 10^{15}cm^{-3}=N_{A\text{-film}}$), fig.4.

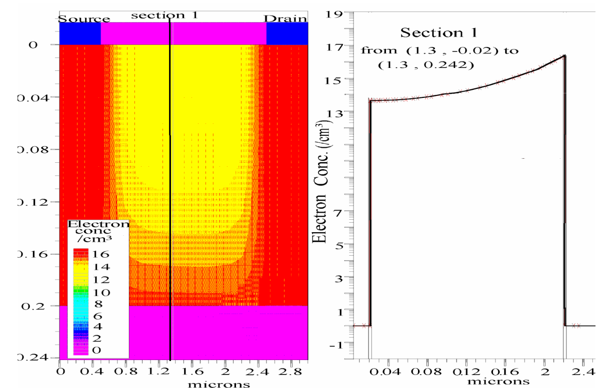


Fig. 4 The electron concentration in the 200nm structure, detail in the film.

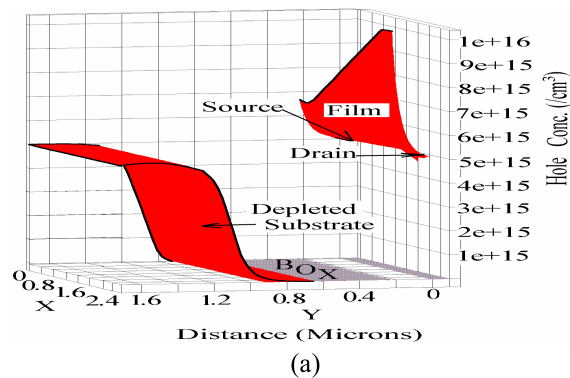
The real effects were taken into account: the interface electric charge in Atlas by the statements:

INTERFACE y.min=0.1 y.max=0.5 QF=5e10

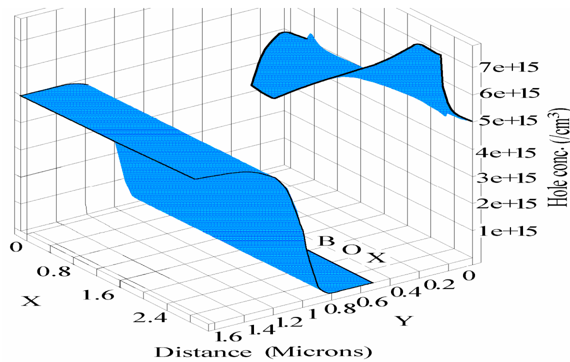
INTERFACE y.min=0.5 y.max=0.8 QF=1e12

This pseudo-MOS transistor has the previous sizes and the doping concentrations in film and substrate N_A=5×10^{15}cm^{-3}. For these doping concentrations the metal-semiconductor work function was Φ_{MS}=-0.32V for the source and drain contacts and zero for the gate contacts, defined as "substrate".

Initially, the following voltages were tried: V_S=0V, V_D=0.3V, V_G=-2.2V. Fig. 5.a presents the holes concentration after ATLAS running. At source, where V_{GS}=-2.2V, the holes reached p=6.5×10^{15}cm^{-3} at the film bottom. At drain, where V_{GD}=-2.5V, the holes reached p=10^{16}cm^{-3}; in both cases higher than the doping concentration N_A=5×10^{15}cm^{-3}. This informs us that the flat-band voltage value, V_{FB}, can be in the -2V vicinity. In a second analysis, the following voltages were applied: V_S=0V, V_D=0.5V, V_G=-1.7V. In this way, the holes concentration at the film bottom reached the value 5×10^{15}cm^{-3}, somewhere in the (x=2µm, y=0.2µm) vicinity, fig.5.b. In order to exactly extract the flat-band voltage, accordingly with the definition, the gate voltage was ramped from -1.9V up to -2V with -0.01V step, monitoring the potential at the film bottom close to source, $\Phi_S=\Phi|_{(0.3,\ 0.2)\mu m}$. When Φ_S=0V the gate voltage was recorded as flat-band voltage. Then, the potential graph was translated with -0.32V value, correcting the metal-semiconductor work function, in order to extract the simulated flat-band voltage, V_{FB}=-1.95V, affected just by the surface electric charges, $Q_{F1,2}$, fig. 6.



(a)



(b)

Fig. 5 The holes concentration in the 200nm pseudo-MOS transistor at: (a) V_S=0V, V_D=0.3V, V_G=-2.2V, (b) V_S=0V, V_D=0.5V, V_G= -1.7V.

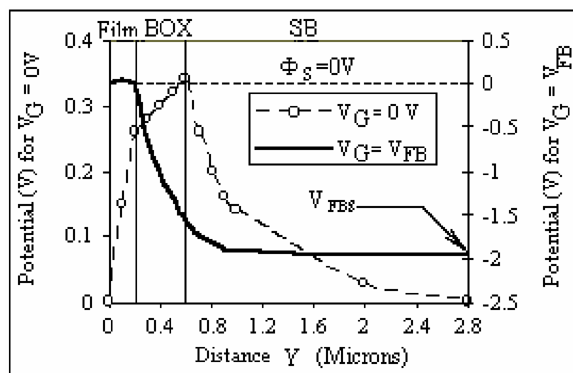


Fig. 6 The V_{FB} extraction, monitoring the gate voltage.

4.2 SOI transistor with 7nm film and vacuum cavity

In this case, $Q_{F1}=10^7$ecm^{-2}, and $Q_{F2}=10^9$ecm^{-2} and the sizes of the structure is available in fig. 7.

The current vectors through the vacuum proved the tunnel effect in the cavity, (black dots in fig. 7) for the nanotransistor with y_{film}=1nm and cavity, at V_D=4V.

The electron concentration from fig.8 reaches a maximum about $6{\cdot}10^{19}$cm^{-3} in the middle of the inversion channel, proving a strong inversion onset, at V_G=3V.

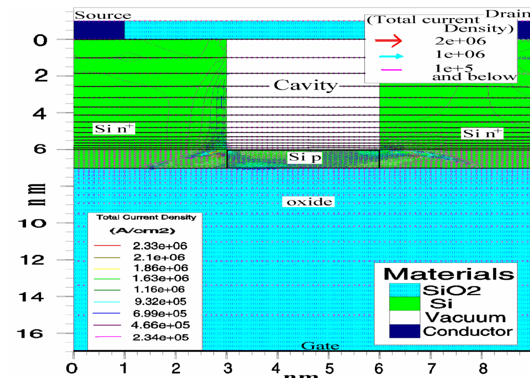


Fig. 7 The current flow through the 7nm structure.

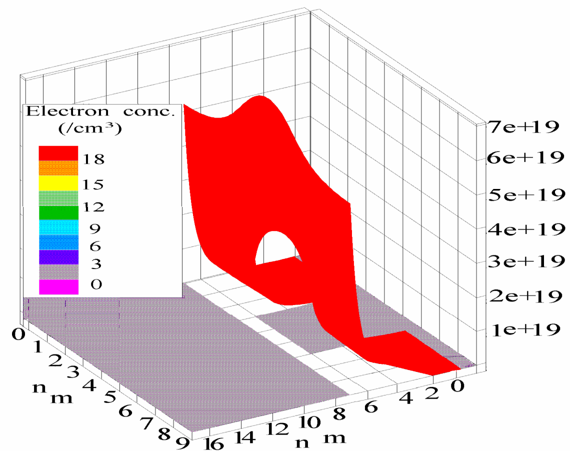


Fig. 8 The electron concentration in the 7nm structure.

4.3 Pseudo-MOS transistor with 2nm film and none undulations

This pseudo-MOS transistor with y_{film}=2nm, y_{ox}=4nm is interesting because the main current is the I_{MOS} current. These sizes represent a theoretical example. For accuracy, the Schrodinger's equation was solved along Ox, Oy axis, including the SCHRO parameter in the MODEL statement:

MODELS conmob srh auger bgn fldmob print schro.

In this case, maximum values were considered: $Q_{F1}=10^{10}$ecm^{-2}, and $Q_{F2}=10^{12}$ecm^{-2}. Essentially, the upper interface is free of charge and the bottom interface is charged just with an elementary electric charge per xOz area, considered 10×10nm^2. Figure 9 proves the V_{FB} estimation. The 2-D holes concentration and 1-D details, respectively section 1 at source (x=0.5nm) and section 2 at drain (x=9.7nm), reveals that V_{FB} belongs to (-0.5,-0.8V). From fig. 9, section 3 is extracted the gate voltage: -1.1V. After a correction by Φ_{MS} value, results V_{FB}=-0.73V. The classical model [6], provide V_{FB}=-0.007V, completely ignoring the bottom interface charge.

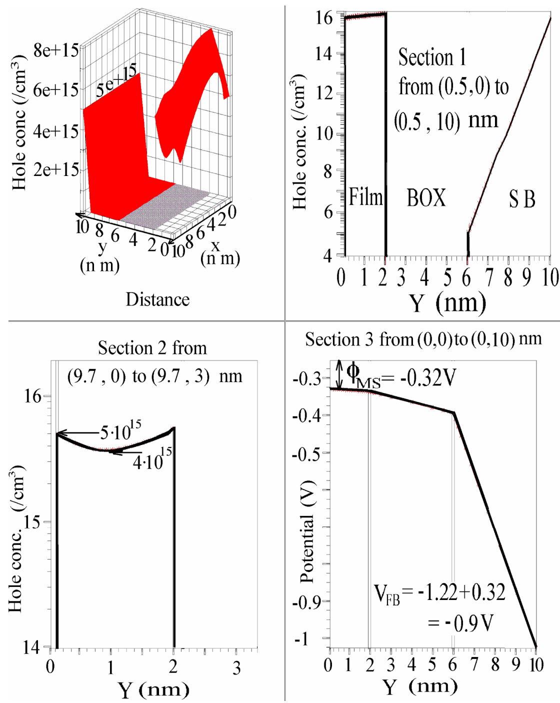


Fig. 9 The simulations results for the 2nm structure.

4.4 SOI transistor with 0.3nm film and vacuum cavity

Despite of the very thin p film, (y_{film}=0.3nm), a high electron concentration occur in the channel at V_G = 3V. As is shown in fig. 10 the I_{MOS} current prevails. The conduction between S – D is ensured through the inversion channel. When V_{DS} increases, the current I_t arises, as a superposition, because the vacuum between source and drain is tunneled.

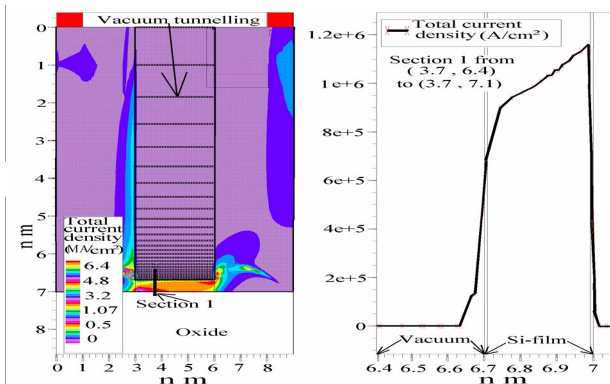


Fig. 10 The total current density in the 0.3nm structure with cavity.

Figure 11 presents the electron concentration in 0.3nm structure (uniatomic Si layer) at V_{DS}=0.1V, V_{GS}=3V, when a strong inversion occurs. The electron concentration in the middle of the channel is: $n=2\cdot10^{20}cm^{-3}=0,2nm^{-3}\approx1$electron per channel volume, V ($V=y_{film}\times x_c\times z_{n+}$= 0,3nm×3nm×6nm=5,4nm^3).

This means that the electron transfer in the uni-atomic Si layer is one by one. Hence, the behavior of this ultra thin SOI nanotransistor with a cavity is similar to a SET (Single Electron Transistor) device.

Another reason to associate these transistors is given by the transfer characteristics for y_{film}=1nm and 0.3nm, having a maximum, like SET [3].

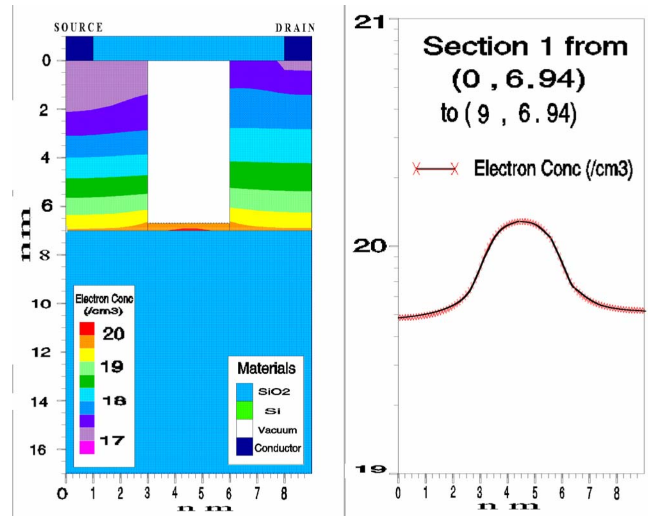


Fig. 11 The electron concentrations in 0.3nm structure.

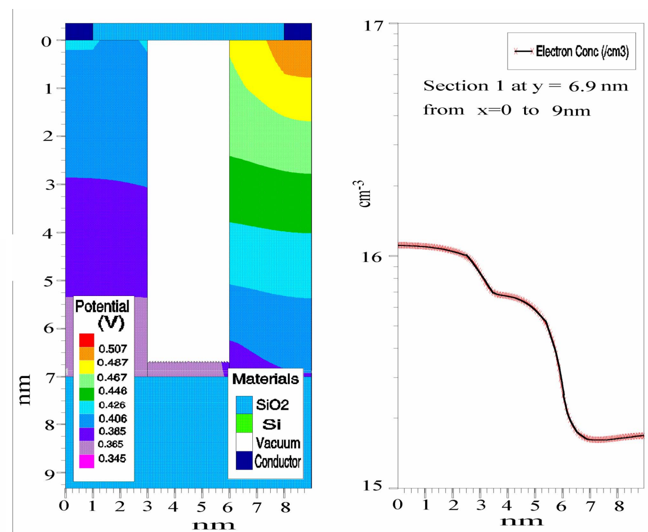


Fig. 12 Potential and electron concentration in 0.3nm structure.

Figure 12 presents the global potential distribution (left) and a detail of the electron concentration (right) for the 0.3nm structure with cavity, biased at a high drain voltage in this last case (V_S=0V, V_G=3V, V_D=4V). The same voltages were applied in fig.7, where the tunnel current density attained just $7\cdot10^5$A/cm^2, while the MOS current density reached $1.2\cdot10^6$A/cm^2. This proved that the tunnel component significantly exists, but less than the inversion channel current, that give the SET like behavior. In this case

the saturation occurred and an unbalanced electron distribution can be seen in the film: $1.1\cdot10^{16}cm^{-3}$ in the source region, $7\cdot10^{15}cm^{-3}$ in the channel near the source, $2\cdot10^{15}cm^{-3}$ in the channel near the drain and decrease up to $1.4\cdot10^{15}cm^{-3}$ in the drain region, at the film bottom.

5 Electrical Characteristics

Figures 13 and 14 comparatively present the simulated static characteristics for all the structures, after ATLAS running. In fig. 13 the family of I_D-V_{DS} curves at V_{GS}=3V, for y_{film}=200nm, 10nm without cavity and 1nm, 0.3nm with cavity is presented. These curves with a minimum prove the tunnel current involvement.

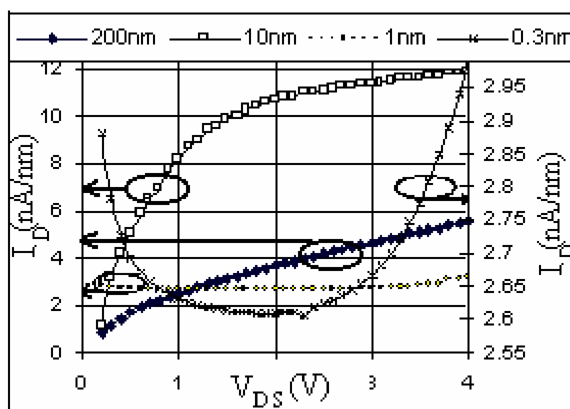


Fig. 13 The I_D-V_{DS} characteristics, at V_{GS}=3V.

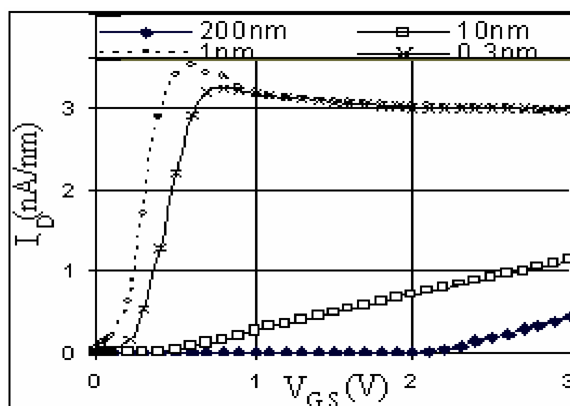


Fig. 14 The I_D-V_{GS} characteristics, at V_{DS}=0.1V.

For I_D–V_{GS} transfer characteristics from fig. 14, the drain voltage was 0.1V, and the gate voltage was increased from 0V to 3V with a 0.05V step. Special characteristics with maximums appeared just for the nanotransistors with cavity.

However the device is in strong inversion at this gate voltage, because $n_{channel}>10^{19}cm^{-3} >>5x10^{15}cm^{-3} = =N_{A\text{-}film}$.

6 Conclusions

A 200nm pseudo-MOS transistor still provides the drain saturation, while the transfer characteristic seems to be close to a SOI-MOSFET commanded by the back-gate.

A sub 7-nm SOI nanotransistor presents quantum effects (e.g. I_D-V_{GS} with a maximum like the SET transistor). The shape of the I_D-V_{DS} curves with a minimum proves the presence of the tunnel effect. Also the electron transfer in the cavity SOI nanotransistor with uni-atomic layer is one by one as in a SET transistor. The nanocavity comprises 1-3 air molecules in normal conditions, negligible for current transport. Consequently this, doesn't imply special vacuum technologies.

A characterization method for the flat-band voltage, using simulation results was presented. If the classical model of the flat-band voltage gives good agreements between analytical-simulation for 200nm Si-film, unfortunately, in the case of sub-10nm film thicknesses there are high discrepancies. The reason is related to the bottom interface that is usually charged at a high level.

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