COMPACT VHDL-AMS SYSTEM LEVEL MODEL OF SMART POWER SWITCHES FOR CONTROL CONCEPT VERIFICATION

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Abstract

This paper presents a method for simulation and experimental verification of compact electro-thermal models for smart power switches. We focus on short circuit events in an automotive environment where high power dissipation and thermal stress severely affect device reliability. For accurate temperature calculation, a compact non-linear thermal network was derived from Z_{th}-curves obtained by non-linear 3D FEM simulations. In this network, we introduced temperature dependent coefficients which are related to the thermal material properties of the smart power device. The electric MOSFET model used was derived from well known SPICE transistor model equations. VHDL-AMS was used to model and simulate the proposed compact electro-thermal power MOSFET model, gate driver and loading conditions. Additionally the simulation results were verified experimentally by combination of both a test chip and a hardware-in-the-loop (HIL) system. The test chip was built in a power technology and consists of power transistors and temperature sensors. The HIL system is a test setup for the laboratory incorporating a FPGA, a compact printed circuit board and a high power DC supply. It is capable to verify thermo-electrical power MOSFET models with arbitrary loading condition and to investigate advanced control concepts. Representative measurements have shown very good correlation with the simulation results which verified the accuracy of the presented approach.

Keywords: Automotive, VHDL-AMS, Compact Modeling, FEM, Smart Power Switch

Presenting Author's biography

H-P Kreuter, graduated in 2007 in Informatics at University of Klagenfurt, Austria, Faculty of Technical Sciences. In 2002 he carried out his diploma thesis at KAI GmbH in Villach, Austria on a topic related to advanced control of pulse stress test systems for smart power switches. He started his PhD in 2008 at TU Vienna, Department of Computer Engineering, and currently works on advanced control and protection concepts for smart power switches.

1 Introduction

Smart power devices are used for switching of high current loads in low-voltage automotive and industrial applications. Protection functions are implemented as analog circuits employing pn-junction based temperature sensors for over temperature shutdown, current measurement with a shunt resistor and op-amps for the over current limitation, as well as a Zener diode clamp circuit protecting the power MOSFET against over-voltages. Over the last decades, these protection concepts have become state of the art.

Advanced analog and digital drive and protection concepts require a method to prove the concept in an early development phase. Thus the overall goal of the presented work was to develop a method to successfully verify such control concepts on a multi-domain system level rather than with a low level mixed-signal simulation. Model development was mainly focused on overload conditions such as shorted loads and transient over-voltage events caused by switching of inductive loads. Power MOSFET test structures with integrated temperature sensors were used to validate the models using a custom designed hardware-in-the-loop test bench.

2 Modeling Approach

VHDL-AMS [1] is used to model the behavior of control concepts and electro-thermal characteristics of power MOSFET transistors and specified loading conditions. Here a VHDL-AMS test bench was created to support the simulation of a shorted load. The block diagram is illustrated in Fig. 1.

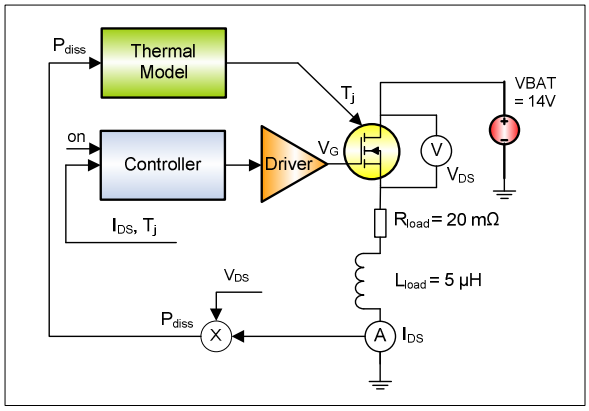

Fig. 1 A typical short circuit scenario

An ideal voltage source *VBAT* represents the battery voltage. The load of the power transistor is modeled using idealized R_{load} and L_{load} elements which represent the impedance of connecting power cables as in the application. Considering the line impedance is important due to the large impact in case of a short circuit event. The thermal model yields the MOSFET junction temperature using the instantaneous power dissipation (P_{diss}). The controller provides protective and switching functions by regulating V_{gs} or I_{gs} respectively.

2.1 Electric MOSFET model

The electric MOSFET model used is derived from well known SPICE transistor model equations. The so-called “Grove-Frohman” model is used in this work. The Grove-Frohman model results in acceptable accuracy and moderate computing costs. Further information on this model may be found in [2].

In case of a short circuit, the chip temperature increases rapidly within a few hundred microseconds to a value exceeding 170°C. This temperature excursion has a significant impact on gain (β) and threshold voltage (V_{th}) of MOSFETs [3]. Therefore, the temperature dependence of these parameters has to be taken into account.

2.2 Compact thermal MOSFET model

It is assumed that heat accumulation and removal from the junction significantly influence the electrical behavior of the power transistor. Here FEM (finite element method) is used to derive the thermal step response directly by transient non-linear 3D thermal simulation. As known from system theory, the step response describes explicitly the transient behavior of linear systems. However, introducing non-linear extensions, it can also serve as a first approximation of the non-linear systems. In case of thermal short at the output (i.e. an ideally cooled backside) a "Foster" network [4] can be used as electrical equivalent of the thermal system and is shown in Fig. 2.

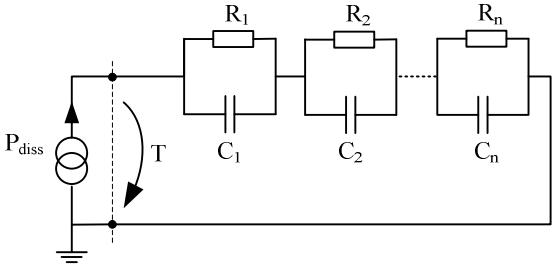

Fig. 2 Thermal Foster network [4]

The simple formal structure of a Foster network leads to a compact mathematical description. The normalized current step response (Z_{th} curve) of an *n*-th order Foster network takes the following form:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{R_i C_i}} \right) \qquad (1)$$

where R_i and C_i are *i*-th thermal resistance and capacitance, respectively. Knowing the Z_{th} curve the RC parameters can be obtained by curve fitting with equation 1. It has to be noted, that in case of the Foster

network, the RC coefficients have no direct connection with the physical parameters of the real object.

So far the thermal model was considered to be linear, temperature independent. Such an approach is usually applied if temperature rise is low (1-10 K). For large temperature deviations the non-linear and temperature dependent material properties, especially of silicon play a significant role [5]. Therefore it is reasonable to implement temperature dependent RC coefficients. A method using power dissipation dependent thermal coefficients is described in [6].

Here the approach is to state a dependence between RC coefficients and simulated temperature. During simulation the instantaneous temperature in the power MOSFET is used to modify the digital filter coefficients. The Z_{th} curves were simulated for different ambient temperatures with constant power dissipation pulses and the corresponding RC coefficients were obtained by equation 1 and by a non-linear ARX (autoregressive with exogenous input) model solved with least squares technique.

For numeric computation of chip temperature based on thermal networks, the analog network was transformed in its digital equivalent. The block diagram of a discrete Foster network is shown in Fig. 3. The filter coefficients a_n and b_n can be calculated from R_n, C_n and Ts as shown in equation 2. Again, R_i and C_i represent thermal resistances and capacitances and Ts is the discrete sampling period.

$$a_n = Ts \cdot \frac{f_{Rn}(Temp)}{1 + f_{Rn}(Temp) \cdot f_{Cn}(Temp) / Ts}$$
$$b_n = \frac{f_{Rn}(Temp) \cdot f_{Cn}(Temp)}{Ts + f_{Rn}(Temp) \cdot f_{Cn}(Temp)} \qquad (2)$$

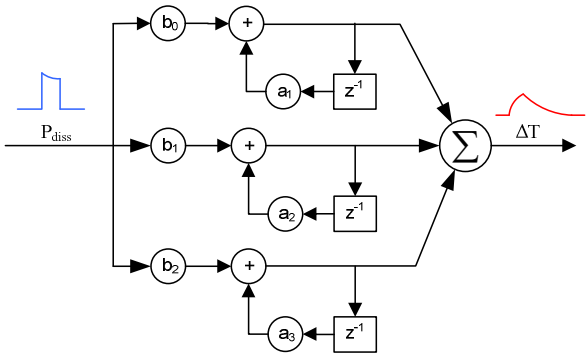

Fig. 3 Block diagram and parameter equations of a discrete Foster network

The temperature dependence of the thermal coefficients can follow different functions and approximations. Exponential functions or power laws are frequently used to model physical effects. Thus, we describe the non-linearity as:

$$R_i = R_{i_0} e^{T-T_0} \text{ and } C_i = C_{i_0} e^{T-T_0} \qquad (3)$$

where R_i and C_i represent the temperature dependent thermal resistances and capacitances and R_{i0} and C_{i0} are the parameters at the reference temperature T_0.

3 Test chip

The schematic of the used test chip is depicted in Fig. 4. The test chip consists of eleven temperature sensors and two vertical power MOSFET transistors having different active areas. The area of the chip is 2.7 x 4 mm^2 and its thickness is about 380 µm. All integrated devices on the test chip are designed in an advanced smart power technology (SPT). This technology allows us to integrate bipolar, CMOS and power MOSFET devices in one chip [7]. Thereby it is possible to integrate accurate temperature sensors using bipolar devices.

Fig. 4 View on the packaged test device (molding compound partially removed above the test chip) [8]

In order to connect all input and output signals, the test chip is assembled in a standard P-DSO-28 plastic package. The electrical connections between pins (leads) and particular structures on the test chip are created by gold wires with a diameter of 50 µm. The drain, source and gate contacts are created on the laterally extruded parts of the power metallization of the power transistors.

The geometrical and FEM model of the test chip was built in the FEM simulator FlexPDE. The geometrical model is depicted in Fig. 5.

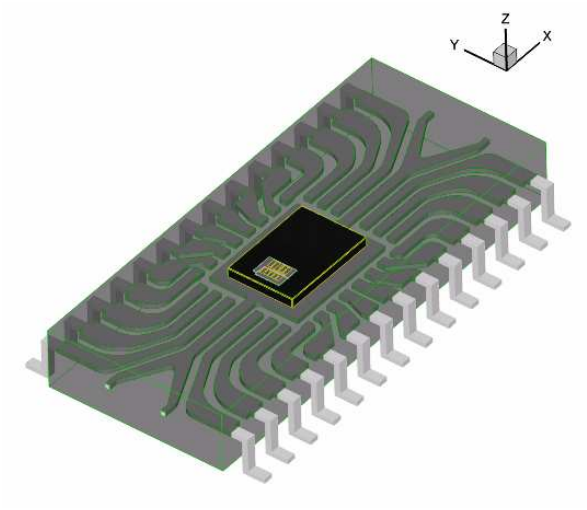

Fig. 5 Geometrical model of the test device for FEM simulation [8]

4 MEASUREMENT SETUP

A hardware-in-the-loop (HIL) system has been developed to investigate digital control and protection concepts and additionally to verify the thermo-electrical power MOSFET models. As controlling unit a standard FPGA device is used. This reconfigurable control device drives the ADCs and DACs of the analog interface named ADDA (analog to digital / digital to analog) as shown in Fig. 6, and it can serve as a prototype target for controller providing arbitrary protection functions.

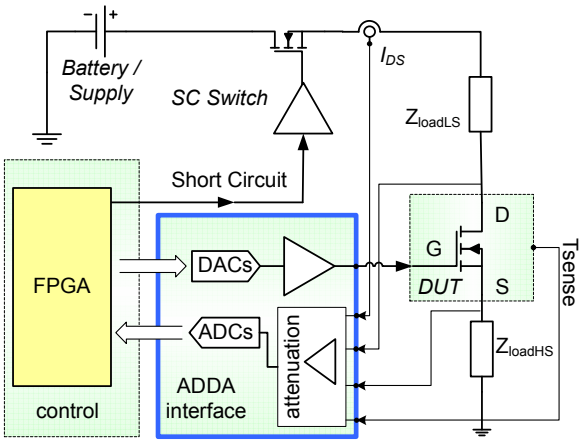

Fig. 6 System architecture of hardware-in-the-loop (HIL) test bench

Facts:

- Digital controlled "bilateral" current source with configurable voltage clamping
- ±10 mA / ±10V current output
- Slew rate: 50 V/µsec
- DAC sample rate: 3 MSpS, 16 bit resolution
- 4 fully differential voltage measurement channels
- Voltage input range: ±60V or ±12V configurable
- ADC sample rate: 2 MSpS with a resolution of 16 bit
- State-of-the-art Flash FPGA with an integrated µC

The gate of the transistor is driven by a digitally controlled current source and the signals from the integrated temperature sensors are acquired by the FPGA device. Variable R_{load} and L_{load} define the real short circuit conditions and a GPIB controlled power supply emulates the battery voltage. V_{GS}, V_{DS}, I_{DS} and up to four temperature sensors are sampled simultaneously. In case of the device failure, e.g. internal drain-source short, the battery voltage is disconnected in less than 2 µsec to prevent any further physical damage.

5 RESULTS

A controller with constant regulation of V_{GS} was implemented with the present HIL test bench. The loading condition was a short circuit with corresponding load resistance of 20 mΩ and cable inductivity of 1e-6 H.

Tab. 1 Test settings

Parameter	Short Pulse	Long Pulse
R_{load}	20 mΩ	20 mΩ
L_{load}	1 µH	1 µH
$Pdissipation_{peak}$	100 W	70 W
$Pulse_{ton}$	125 µsec	6 msec
T_{start}	25 °C	-40 °C

The test settings are listed in Tab.1. We used representative test pulses with two different pulse widths and start temperatures.

First we implemented the linear thermal model with constant *R* and *C* coefficients. The simulation and experimental results are shown in Fig. 7. The simulated behavior of the short pulse deviates from the measurements, but the difference is acceptable. However, in the case of the long pulse, the maximum deviation is as large as 20% and results to significant model errors.

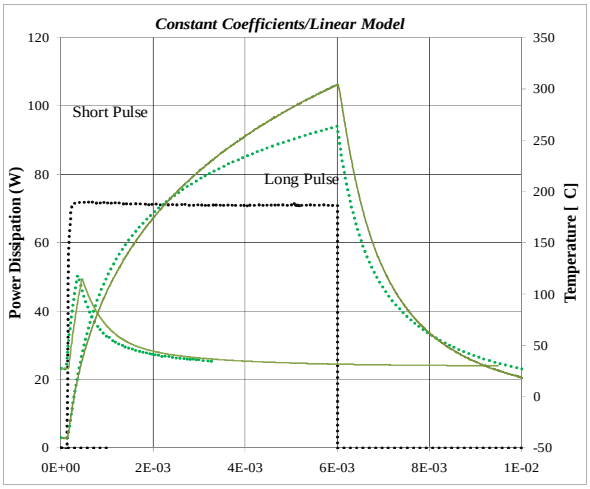

Fig. 7 Simulated (solid line) and measured (dashed line) behavior during short circuit using the linear thermal network.

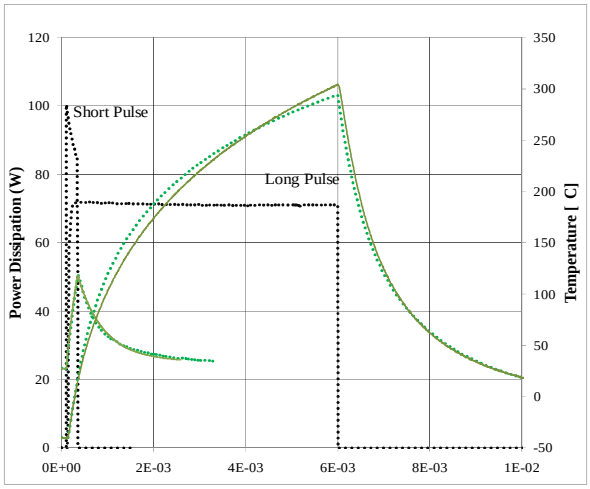

Fig. 8 Simulated (solid line) and measured (dashed line) behavior during short circuit using the non-linear thermal network.

In the second approach the non-linear thermal network was applied to simulate the device temperature. We used the same experimental test settings for the simulation of the short and long pulse. The simulation and experimental results are shown in Fig. 8. The simulated behavior for both test cases agrees very well with the measured one. A maximum relative deviation of about 5 % was observed, which is acceptable for concept verification on system level.

Tab. 2 Simulation runtimes

Simulator	Simulation Runtime
FEM (FlexPDE)	2-4 h
VHDL-AMS (Cadence AMS Designer)	few seconds

The simulation runtime of the FEM simulation was 2 to 4 hours, as listed on Tab. 2, on a standard workstation with 4 cores operating at 2.5 GHz with 8 GB RAM. The VHDL-AMS simulation took only a few seconds with identical hardware setup, yielding to a significant acceleration of the transient electro-thermal simulation. With this approach, we are able to run fast system-level simulations with significantly increased accuracy.

6 Outlook and Conclusion

The presented behavioral modeling approach can be used to develop and optimize control and protection concepts of smart power devices under applicative conditions with very good accuracy while significantly reducing the simulation effort due to compact models implemented in VHDL-AMS. The presented models were verified on a special HIL test system and special test chips with integrated temperature sensors. We introduced a non-linear thermal network which yields to a significantly increased accuracy while preserving short simulation runtimes.

7 Acknowledgement

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